ABSTRACT OF THE DISCLOSURE

[1117] A three-dimensional memory array includes a plurality of rail-stacks on each of several levels forming alternating levels of X-lines and Y-lines for the array. Memory cells are formed at the intersection of each X-line and Y-line. The memory cells of each memory plane are all oriented in the same direction relative to the substrate, forming a serial chain diode stack. In certain embodiments, row and column circuits for the array are arranged to interchange function depending upon the directionality of memory cells in the selected memory plane. High-voltage drivers for the X-lines and Y-lines are each capable of passing a write current in either direction depending on the direction of the selected memory cell. A preferred bias arrangement reverse biases only unselected memory cells within the selected memory plane, totaling approximately N^2 memory cells, rather than approximately $3N^2$ memory cells as with prior arrays.